

5

SYSTEM AND METHOD FOR ADDRESSING MEMORY AND TRANSFERRING DATA

10

Abstract

A system and method for addressing memory and transferring data, which in some embodiments include one or more processor translation look-aside buffers (TLBs) and optionally one or more I/O TLBs, and/or a block transfer engine (BTE) that optionally includes a serial cabinet-to-cabinet communications path (MLINK). In some embodiments, the processor TLBs are located within one or more common memory sections, each memory section being connected to a plurality of processors, wherein each processor TLB is associated with one of the processors. The BTE performs efficient memory-to-memory data transfers without further processor intervention. The MLINK extends the BTE functionality beyond a single cabinet.

15

20

"Express Mail" mailing label number: EL671642534US

Date of Deposit: October 24, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

25